Claims

[c1] 1. A digital DC bias estimation apparatus for estimating a DC bias of a received signal obtained from sampling a received packet, wherein the digital DC bias estimation apparatus comprises:

a symbol boundary detection unit for differentiating the received signal to obtain a differential curve, slicing the differential curve into a sliced binary comparison base signal by assigning a starting point on a region beyond a transition setting threshold range in the differential curve as a transition point, and issuing a boundary signal when the transition is occurred;

a preamble pattern identification enabling unit for counting a sampling number between the contiguous boundary signals wherein the counted sampling number is reset to zero each time when the boundary signal is occurred, and issuing a preamble pattern storing signal before the counted sampling number reset to zero is within an allowable range;

a preamble pattern identification unit for obtaining the sliced binary comparison base signal according to the preamble pattern storing signal, comparing the continuously obtained sliced binary comparison base signals

with a predefined preamble pattern, and issuing a matching signal when the pattern of the sliced binary comparison base signals matches the predefined preamble pattern; and

a bias calculation unit electrically coupled to the preamble pattern identification unit for outputting an average potential of peaks of each bit of the received signal, which is corresponded to the sliced binary comparison base signal that matches the predefined preamble pattern before the matching signal appears, as an estimated DC bias.

[c2] 2. The digital DC bias estimation apparatus of claim 1 wherein the symbol boundary detection unit further comprises:

a noise eliminator for differentiating the received signal to obtain the corresponding differential curve, and moving averaging a plurality of curve values that are contiguous in the differential curve, so as to output an averaged differential curve;

a distortion alleviator for outputting an original value of the averaged differential curve when the averaged differential curve is beyond the transition setting threshold range, and outputting a previously output value when the averaged differential curve is within the transition setting threshold range, so as to form a distortion allevi-

ated signal;
a slicer for slicing the distortion alleviated signal and generating the sliced binary comparison base signal; and
a transition detection unit for outputting the boundary signal when the transition of the sliced binary comparison base signal is occurred.

[c3] 3. The digital DC bias estimation apparatus of claim 1 wherein the preamble pattern identification enabling unit further comprises:
a first counter for counting the sampling number between the contiguous boundary signals, resetting the sampling number to zero and outputting a counting zero signal each time when the boundary signal is occurred, and outputting a bit enabling signal when the counted sampling number is within an allowable range before it is reset to zero; and
an AND gate in which the counting zero signal, the bit enabling signal, and the boundary signal are input for operating the input signals and outputs the preamble pattern storing signal.

[c4] 4. The digital DC bias estimation apparatus of claim 3 wherein the preamble pattern identification enabling unit further comprises:
a second counter for counting the number of the boundary signals, and enabling the AND gate when the number

of the boundary signals reaches a predetermined number.

[c5] 5. The digital DC bias estimation apparatus of claim 1 wherein the preamble pattern identification unit further comprises:
a shift register for storing the sliced binary comparison base signal record by record according to the preamble pattern storing signal; and
a pattern matching unit electrically coupled to the shift register for comparing the predefined preamble pattern with the data stored in the shift register.

[c6] 6. The digital DC bias estimation apparatus of claim 1 wherein the bias calculation unit further comprises:
a first shift register for storing and outputting the received signal record by record according to the preamble pattern storing signal; and
a bias estimation unit electrically coupled to the first shift register for obtaining and calculating an average value of the peaks of the received signals output from the first shift register according to the matching signal, so as to obtain the estimated DC bias.

[c7] 7. The digital DC bias estimation apparatus of claim 6 wherein the bias calculation unit further comprises:
a peak searching unit electrically coupled to the first

shift register for obtaining a peak of the received signal stored in the first shift register during a period from the previous time of the preamble pattern storing signal enabling the shift register to the current time of the preamble pattern storing signal enabling the shift register according to the preamble pattern storing signal, and outputting the peak;

wherein, the bias estimation unit calculates an average value of the peaks in the received signal corresponded to the sliced binary comparison base signal that matches the predefined preamble pattern, so as to obtain the estimated DC bias.

[c8] 8. The digital DC bias estimation apparatus of claim 7 wherein the bias calculation unit further comprises:

a second shift register electrically coupled to the peak searching unit for storing the peak output from the peak searching unit record by record according to the preamble pattern storing signal, and for outputting the stored peaks record by record in an appropriate timing.

[c9] 9. The digital DC bias estimation apparatus of claim 1, further comprising:

a correlation unit for subtracting the estimated DC bias from the received signal to obtain an bias-reduced received signal, performing a correlation operation on the bias-reduced received signal and a predefined correla-

tion signal, and outputting a trailer bit enable signal when the value obtained from the correlation operation is beyond a trailer setting threshold range; and
a trailer bias estimation unit for calculating an average value of the samples of the received signal corresponding to the trailer bit, and outputting the calculation result as a trailer DC bias.

[c10] 10. A digital DC bias estimation method for estimating a DC bias of a received signal obtained from sampling a received packet wherein the digital DC bias estimation method comprises:
differentiating the received signal to obtain a differential curve;
slicing the differential curve into a sliced binary comparison base signal by assigning a starting point on a region beyond a transition setting threshold range in the differential curve as a transition point, and issuing a boundary signal when the transition is occurred;
counting a sampling number between the contiguous boundary signals wherein the counted sampling number is reset to zero each time when the boundary signal is occurred;
obtaining the sliced binary comparison base signal in the comparison base signal during a corresponding period when the counted sampling number is reset to zero

within an allowable range;
comparing the continuously obtained sliced binary comparison base signals with a predefined preamble pattern, and obtaining an average value of the peaks in each bit period of the received signal corresponded to the comparison base signal that matches the predefined preamble pattern before the matching signal appears, and outputting the average potential as an estimated DC bias.

[c11] 11. The digital DC bias estimation method of claim 10, further comprising:
subtracting the estimated DC bias from the received signal to obtain an bias-reduced received signal;
performing a correlation operation on the bias-reduced received signal and a predefined correlation signal, and outputting a trailer bit enable signal when the value obtained from the correlation operation is beyond a trailer setting threshold range; and
calculating an average value of the received signal at a synchronization sampling point according to the trailer bit enable signal, and outputting the calculation result as a trailer DC bias.